



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/824,907 | 04/15/2004 | Yushi Jinno | YKI-0150 | 7608 |
| 23413 | 7590 | 03/17/2006 | EXAMINER | |
| CANTOR COLBURN, LLP 55 GRIFFIN ROAD SOUTH BLOOMFIELD, CT 06002 | | | TRAN, LONG K | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2818 | |

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/824,907

Applicant(s)

JINNO, YUSHI

Examiner

Long K. Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 9-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group I** (claims 1 – 8) in the reply filed on 01/12/2006 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on 04/15/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1, 3, 4, 5, 6 and 8** are rejected under 35 U.S.C. 102(e) as being e by anticipated by Matsunaga et al. (US Patent No. 6,873,174).

Regarding claim **1**, Matsunaga discloses (figs 16 – 19) method of manufacturing an active matrix display panel which comprises, for each pixel a display element and a thin film transistor for controlling connection between the display element and a power source line, the method comprising the steps of:

thin film transistor (14,1102) formed on a substrate (11,1100), therefore, Matsunaga teaches the method of forming ; and

Art Unit: 2818

after formation of the thin film transistor, a plurality of layers accumulated to complete formation of the display element, therefore, Matsunaga teaches the method of forming

wherein

the step of accumulating a plurality of layers includes at least one step of forming a planarization insulating film (998,199; Examiner modified fig. 18') having a large thickness and an insulating property, and

the method further comprises, prior to the at least one step of forming a planarization insulating film (998,19; Examiner modified fig. 18'), a step of disconnecting a line between the display element and the power source line with regard to a defective pixel (column 20, lines 50 – 67).

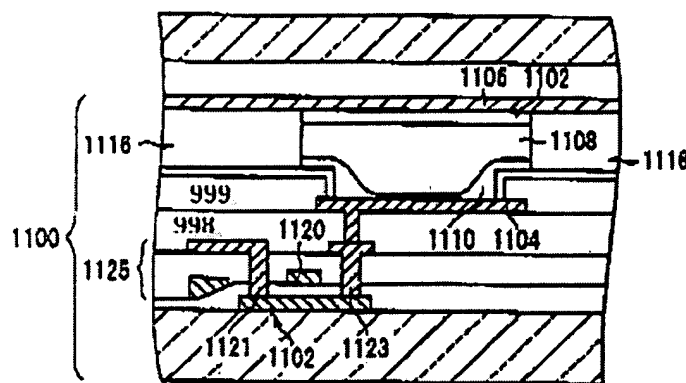


FIG. 18'

Regarding claim 3, Matsunaga discloses the display is an organic electroluminescence (column 20, lines 33 – 34).

Regarding claim 4, Matsunaga discloses (figs 16 – 19) method of manufacturing an active matrix display panel which comprises, for each pixel a display element and a

Art Unit: 2818

thin film transistor for controlling connection between the display element and a power source line, the method comprising the steps of:

thin film transistor (1102) formed on a substrate (1100), therefore, Matsunaga teaches the method of forming;

forming a gate electrode (1120) of the thin film transistor (1102) and a line (1121) for the gate electrode;

forming source and drain electrodes of the thin film transistor (1102) and a line for connecting one of the source and drain electrodes to the power source line (1121);

connecting the power source line to a power source, controlling (900, fig 16) application of a signal to the gate electrode of the thin film transistor, and performing a continuity test by detecting the state of the electrode which is not connected to the power source line in accordance with an switching operation (SW1 –SW3, fig 16) of the thin film transistor; and

with regard to a pixel which is determined by the continuity test to be defective, disconnecting a line between the display element and the power source line via the thin film transistor,

wherein

the continuity test and the line disconnection is performed prior to completion (column 20 lines 50 – 60) of formation of the display element.

Regarding claim 5, Matsunaga discloses the continuity test is performed after one electrode of the display element is formed (column 20, lines 40 – 60).

Art Unit: 2818

Regarding claim 6, Matsunaga discloses a step of forming an insulating film having planarity after the continuity test and the line disconnection (column 20, line 50 – 60),

Wherein a concave portion generated at the time of the line disconnection is repaired by the insulation.

Regarding claim 8, Matsunaga discloses the display is an organic electroluminescence (column 20, lines 33 – 34).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsunaga et al. (US Patent No. 6,873,174) as applied to claim 1 or 4 above, and further in view of Shiota et al. (US Patent Application Publication No. 2002/0154079).

Regarding claims 2 and 7, Matsunaga discloses the claimed invention of claim 1 or 4 except for the disconnection is performed by laser irradiation.

However, it is known in the art that laser irradiation is used to connect or disconnect defective pixel also shown by Shiota ([0019]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to laser irradiation for disconnection of defective pixels in Matsunaga as taught by Shiota, since it was known

Art Unit: 2818

in the art that using laser irradiation for disconnect and connect defective pixels is easy with low cost.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT



March 17, 2006